Code: 9A04502

R09

B.Tech III Year I Semester (R09) Regular & Supplementary Examinations December 2014

LINEAR IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

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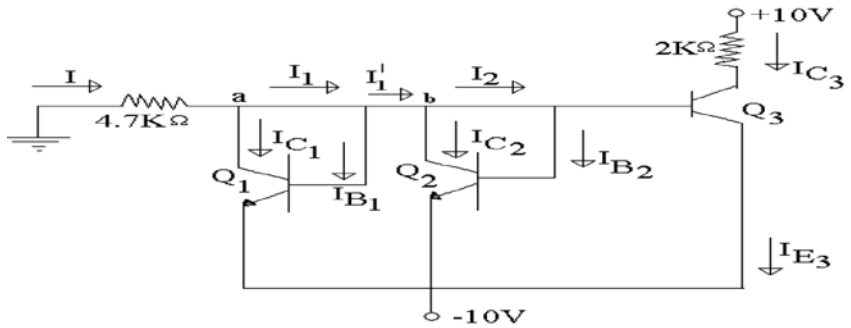
1 (a) Determine the emitter current in transistor Q_3 of figure. If V_{BE} = 0.7 V and β = 100.



(b) Discuss the differences between the differential amplifiers used in the first two stages of op - amp.

2 (a) List out the ideal characteristics of an OP-AMP.

(b) What is an OP-AMP? Why it is called so?

(c) Why is it desirable for an op-amp to have a high CMRR?

3 (a) Using an Op-Amp powered from ± 15 V regulated supplies, design a photo detector amplifier such that as i_1 changes from 0 to 1 μA, V_o changes form -5 V to +5 V. What is the minimum open-loop gain for a deviation of the transfer characteristics from the ideal of < 1%?

(b) List out the advantages of instrumentation amplifier.

4 (a) What feedback is preferred for oscillators and why? What is the effect of negative feedback?

(b) Derive the frequency of oscillation of a RC phase shift oscillator and explain the operation of the circuit.

5 (a) Explain the operation of first order high pass buffer worth filter.

(b) Design a HPF at the cutoff frequency of 1 kHz and a pass band gain of 2.

6 (a) Draw the block schematic of a PLL describing the function of each block briefly.

(b) What is the purpose of law pass filter in a phase locked loop? Describe different types of law pass filters used in a PLL.

7 (a) Explain the operation of an op-amp based weighted resistor digital to analog converter through a neat circuit diagram.

(b) Design a 4-bit weighted resistor DAC whose full-scale output voltage is –10 Volts. Assume R_f = 10 k and logic '1' level as +5 volts. And logic '0' level as 0 volts. What is the output voltage when the input is 1011?

8 Derive the output voltage expression for:

(a) Analog voltage multiplier circuit.

(b) Analog voltage divider circuit.

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